

Customer No.: 31561  
Application No.: 10/604,613  
Docket No.: 11039-US-PA

### AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

#### Listing of Claims:

Claims 1-12 (withdrawn).

13. (currently amended) A multi-level SONOS memory cell, comprising:

a substrate, comprising:

a substrate layer;

an insulation layer, disposed on the substrate layer;

a silicon stripe, disposed on the insulation layer;

~~a first two discrete control gates gate and a second control gate~~ disposed respectively on sidewalls of the silicon stripe;

source/drain regions, configured in the silicon stripe beside both sides of the ~~first control gate and the second two discrete control gates gate~~; and

~~two a silicon oxide/silicon nitride/silicon oxide composite layers layer~~, disposed between the ~~first two discrete control gates gate~~ and the silicon stripe, ~~and between the second control gate and the silicon stripe respectively.~~

14. (original) The memory cell of claim 13, wherein the substrate comprises a silicon-on-insulator substrate.

15. (currently amended) A multi-level memory cell, comprising:

a substrate;

an insulation layer, disposed on the substrate;

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a semiconductive stripe, disposed on the insulation layer;

~~a first two discrete control gates gate and a second control gate~~ disposed respectively on sidewalls of the semiconductive stripe;

source/drain regions, configured in the semiconductive stripe beside both sides of the two control gates ~~first conductive gate and the second conductive gate~~;

~~two~~ a charge trapping ~~layer layers~~, disposed between the two discrete first control gates gate and the semiconductive stripe respectively, ~~and between the second control gate and the semiconductive stripe~~;

~~two~~ a first dielectric ~~layer layers~~, disposed between the two charge trapping layer layers and the semiconductive stripe respectively; and

~~two~~ a second dielectric ~~layer layers~~, disposed between the two charge trapping layer layers and the two discrete first control gates respectively ~~gate, and between the charge trapping layer and the second control gate~~.

16. (original) The multi-level memory cell of claim 15, wherein the semiconductive stripe comprises silicon.

17. (currently amended) The multi-level memory cell of claim 15, wherein the two charge trapping layer layers comprises a silicon nitride ~~layer layers~~.

18. (currently amended) The multi-level memory cell of claim 15, wherein the two first dielectric layer layers comprises a silicon oxide ~~layer layers~~.

19. (currently amended) The multi-level memory cell of claim 15, wherein the two second dielectric layer layers comprises a silicon oxide ~~layer layers~~.